Monolithic Two-Tier Dual Gated Ga-doped In_2O_3 1T-1C Memory Cell for Bit Cost Scalable 3D FeRAM

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Ferroelectric Hafnium-Zirconium-Oxide (HZO) memories have recently emerged as promising refresh-free RAM solutions [1]. Among them, the one-transistor–one-capacitor (1T1C) FeRAM offers robust endurance, retention, low-voltage operation, and scalability. To address growing AI-driven memory demands, BEOL-compatible monolithic 3D stacking enables higher densities with minimal footprint. Bit-cost scalable designs are key for practical 3D integration. Amorphous oxide semiconductor (AOS) MOSFETs, such as indium tungsten oxide (IWO) [2] or indium gallium oxide (IGO), offer BEOL compatibility, ultra-low off-current, high mobility, strong electrostatic control, and suitability for advanced architectures, making them strong candidates for 3D 1T1C FeRAM access devices.

We present a compact 3D integration of vertically stacked 1T1C ferroelectric memory (FeRAM) cells, as illustrated in Fig. 1(a–b), featuring common gate architecture and vertical bit-line (VBL) connectivity for enhanced scalability. The cross-sectional STEM images (Fig. 1(c–d)) and EDS mapping (Fig. 1(e)) confirm successful stacking of dual-gate (DG) MOSFETs and ferroelectric capacitors (FeCAPs), utilizing 5 nm HZO and ~800 nm gate lengths. The DG MOSFETs employ gallium-doped indium oxide (IGO) channels with 18% Ga doping, fabricated via an ALD super-cycle process (1 Ga cycle per 4 In_2O_3 cycles). Electrical characterization of FeCAPs in Tier 1 and Tier 2 reveals minor loop P-V behavior (Fig. 1(f)), pulse-width-dependent switching dynamics (Fig. 1(g)), and endurance under 100%, 50%, and 75% switching conditions (Fig. 1(h)). Transfer characteristics (Fig. 1(i)) demonstrate independent threshold voltage (V_T) modulation via control gates, while output curves (Fig. 1(j)) show clear current saturation and high I_{on}, confirming the suitability of this architecture for high-performance 3D FeRAM applications. Fig. 2 illustrates the functional and simulated performance of the proposed 3D-stacked 1T1C FeRAM architecture. The write scheme (Fig. 2(a)) applies tier-specific voltages (0.8 V, 1.4 V, 2.0 V) to the bit-line (BL) with grounded plate-line (PL) for writing '1', and reverses polarity for writing '0', with monotonic BL current confirming successful programming. Destructive read operations (Fig. 2(b)) ramp PL from 0.4 V to 2.0 V in 0.2 V steps following a -2 V pre-erase, validating read accuracy across tiers. Polarization versus read voltage data (Fig. 2(c)) shows strong ferroelectric response (>40 μC/cm² above 1.2 V), while retention measurements (Fig. 2(d)) demonstrate stability up to 10^4 s at 25°C, with projections extending to 10 years. TCAD mixed-mode simulations (Fig. 2(e–j)) model the stacked DG IGO MOSFETs and MFM capacitors, with calibrated results (Fig. 2(f)) matching experimental data. Scaled projections (Fig. 2(g)) indicate high I_{on} (186 μA) and low I_{off}, and simulated sensing waveforms (Fig. 2(h–j)) confirm reliable readout of both 'Data 1' and 'Data 0', supporting the architecture's feasibility for robust 3D FeRAM operation.

References

[1] N. Ramaswamy et al., "NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads," 2023 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2023.

[2] S. Datta et al., "Amorphous Oxide Semiconductors for Monolithic 3D Integrated Circuits," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024.

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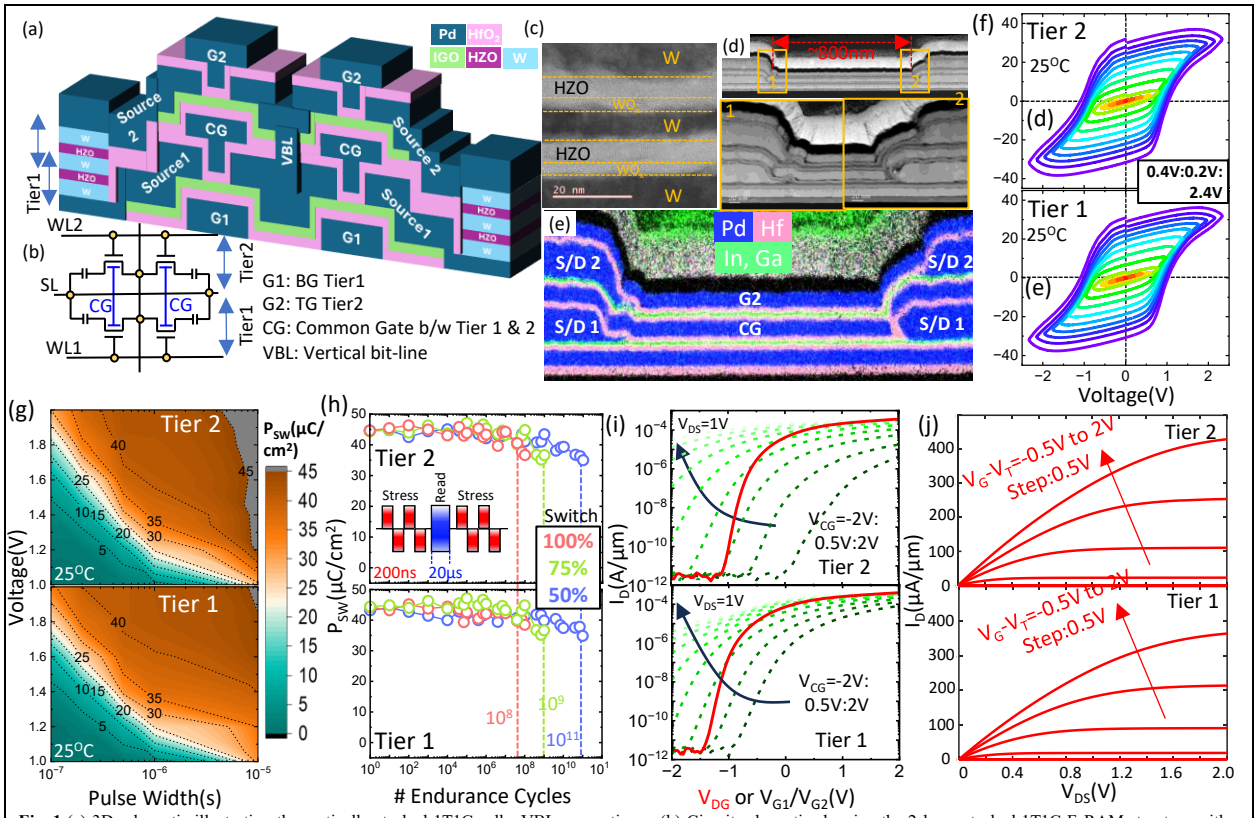

Fig. 1 (a) 3D schematic illustrating the vertically stacked 1T1C cells, VBL connections; ;(b) Circuit schematic showing the 2-layer stacked 1T1C FeRAM structure with common gates and vertical bit-lines for compact integration; (c) Cross-sectional STEM of 2-stacked FE CAPs with 5 nm HZO; (d) STEM of 2-stacked DG IGO MOSFET showing ~800 nm gate length; (e) EDS mapping confirms element locations and successful stacking of 2 DG MOSFETs; (f) Minor loop P-V characteristics of ferroelectric capacitors (FeCAPs) in Tier 1 and Tier 2; (g) Pulse-width-dependent switching behavior of FeCAPs in both tiers. (h) Endurance characteristics of 2-stacked FeCAPs under 100%, 50%, and 75% switching conditions; Vertically stacked DG MOSFETs using gallium-doped indium oxide (IGO) channels with 18% Ga doping, fabricated via ALD super-cycle process (1 Ga cycle per 4 In_2O_3 cycles); (i) Transfer characteristics of Tier 1 and Tier 2 MOSFETs, where independent control of the CG enables V_T modulation. Devices with DG operation exhibit enhanced performance with tunable V_T; (j) Output characteristics of the DG MOSFETs showing clear current saturation and high I_{ON}, demonstrating suitability for 3D FeRAM applications.

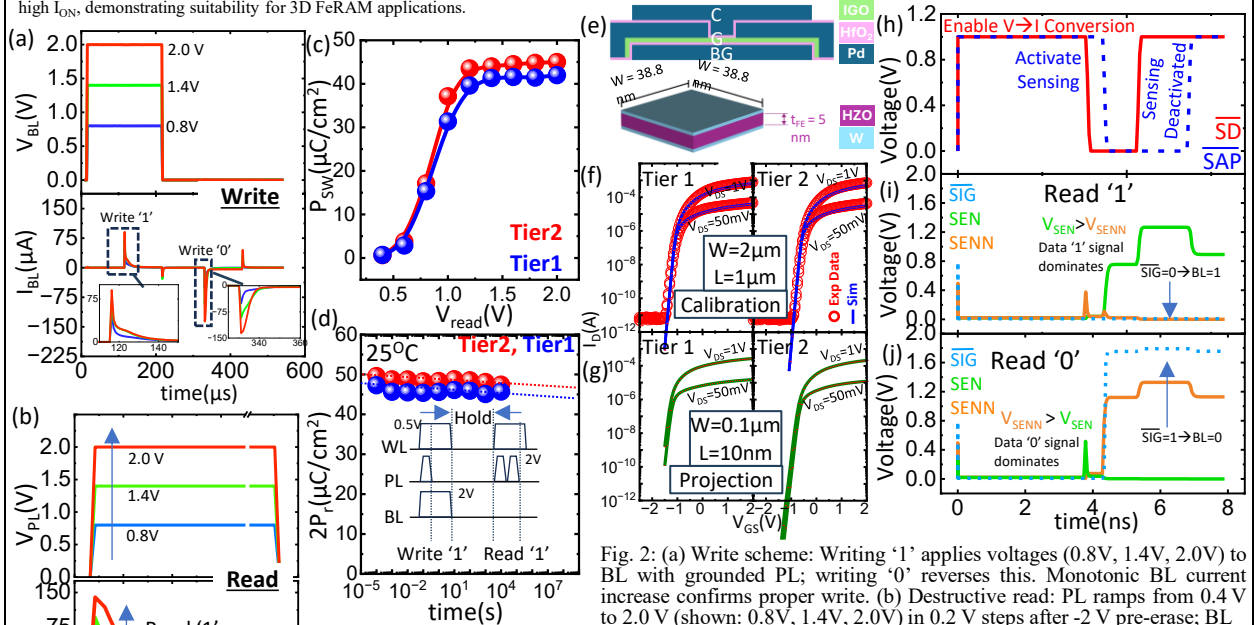

Fig. 2: (a) Write scheme: Writing '1' applies voltages (0.8V, 1.4V, 2.0V) to BL with grounded PL; writing '0' reverses this. Monotonic BL current increase confirms proper write. (b) Destructive read: PL ramps from 0.4 V to 2.0 V (shown: 0.8V, 1.4V, 2.0V) in 0.2 V steps after -2 V pre-erase; BL current validates correct read across tiers. (c) Polarization vs. read voltage shows >40 μC/cm² above 1.2 V, indicating strong readout. (d) Retention of Tier 1 and 2 cells measured up to 10^4 s at 25°C, projected to 10 years. TCAD mixed-mode simulation analyzes 3D-stacked 1T1C FeRAM with DG IGO transistors and MFM capacitors. (e) Schematic shows stacked DG IGO MOSFET and capacitor. (f) Model calibration matches experimental data. (g) Scaled performance projects ION = 186 μA and low IOFF. (h) Simulated sensing waveform using adapted sense amplifier. (i-j) Readout simulations confirm successful sensing of 'Data 1' and 'Data 0'.